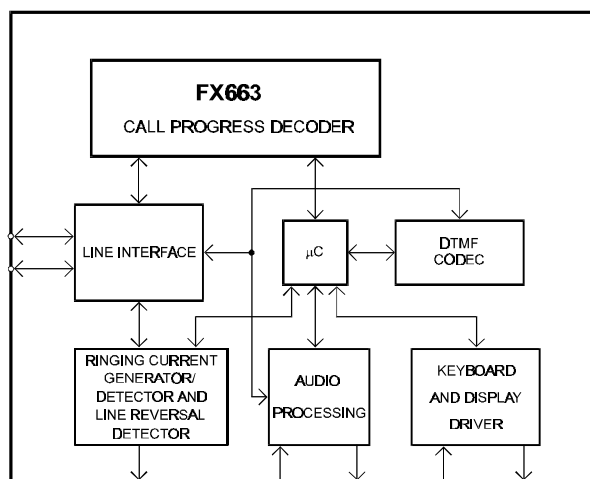


1.0 Features

- **Decodes Call Progress Tones Worldwide covering:**
 - **Single and Dual Tones**
 - **Fax and Modem Answer/Originate Tones**
 - **Special Information Tones**
 - **Fast 'US Busy' Tone Detector**
- **Low-Power (3 Volt) Operation**
- **Adjustable Detection Threshold**
- **Voice Detector**
- **Standard 3.58MHz Xtal/Clock Input**
- **16-Pin SOIC and DIP Packages**



1.1 Brief Description

The FX663 decodes the standard audible tone signals provided by telecom systems worldwide to indicate Dial, Ringing, Busy, Unobtainable and other stages of a call attempt. It provides the key features needed for intelligent, full-function, call progress monitoring by applications involving machine dialling or automatic call placement. The FX663 also incorporates the following features:

- Single and dual tone decoding for better cross-system Call Progress monitoring.
- "US Busy" tone detector, saving time needed for "cadence verification" under Busy and Unobtainable conditions. This incorporates a separate 620Hz detector for improved response.
- A detector to indicate speech and non-call progress signals; this reduces voice falsing of call progress tones and adds Voice-Answer detection as a "connected" prompt.
- A fax and modem tone decoder.
- A separate, adjustable threshold, signal-level detector which reduces noise falsing.

The FX663 uses new digital signal processing techniques to provide these advantages. It is a low cost, low power product with superior performance. It is available in industry standard 16-pin packages.

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1.2 Block Diagram

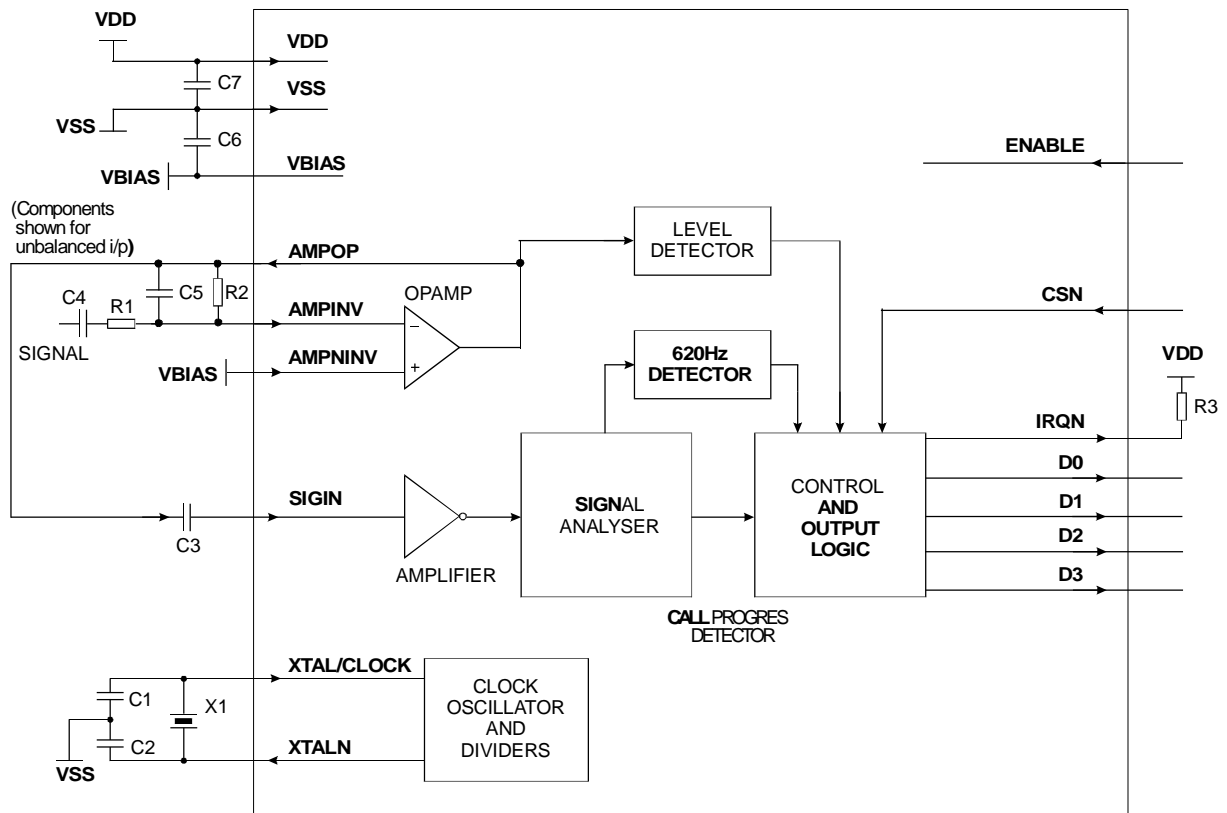


Figure 1 Block Diagram

1.3 Signal List

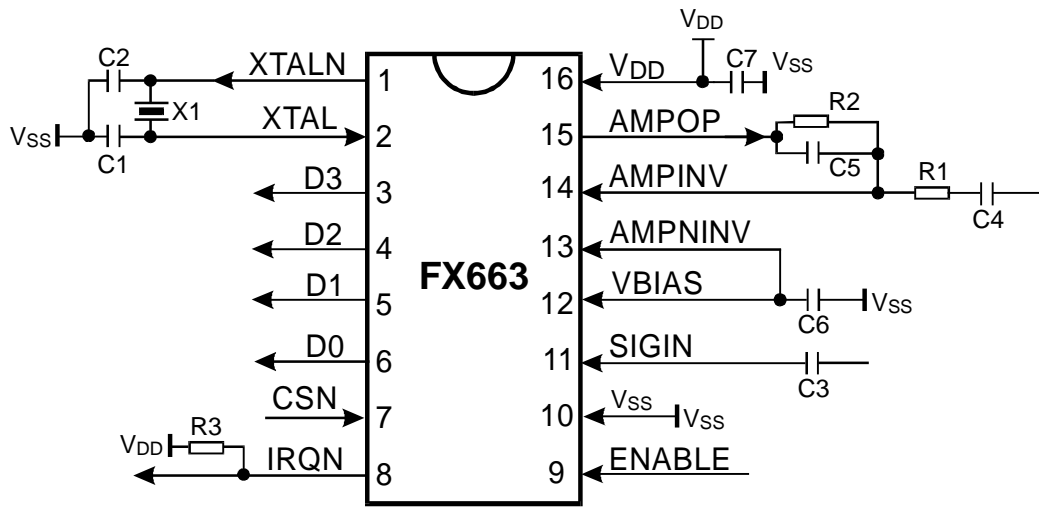
Package D4/P3	Signal		Description
Pin No.	Name	Type	
1	XTALN	O/P	The inverted output of the on-chip oscillator.
2	XTAL/CLOCK	I/P	The input to the on-chip oscillator, for external Xtal circuit or clock.
3	D3	O/P	D3, D2, D1 and D0 is a 4-bit parallel data word output to the μ Controller. The transmission of data is under the control of the CSN input. These 3-state outputs are held at high impedance when CSN is at "1". See Bus Timing Diagram (Figure 8). If CSN is permanently at "0", D3, D2, D1 and D0 are permanently active. See Timing Diagram (Figure 4 to 7).
4	D2	O/P	
5	D1	O/P	
6	D0	O/P	
7	CSN	I/P	The data output control function: this input is provided by the μ Controller. Data transfer sequences are initiated, completed or aborted by the CSN signal. See Bus Timing Diagram (Figure 8).
8	IRQN	O/P	This output indicates an interrupt condition to the μ Controller by going to a logic "0". This is a "wire-ORable" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the μ Controller. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pullup resistor is required. If CSN is permanently at "0", the interrupt condition is a logic "0" pulse. See Timing Diagram (Figure 4 to 7).
9	ENABLE	I/P	A low level input selects the powersave mode, all circuits are reset and disabled. D0 - D3 outputs become high impedance. A high level enables all circuits. (See also CSN).

1.3 Signal List (continued)

Package D4/P3	Signal		Description
Pin No.	Name	Type	
10	V _{SS}	Power	The negative supply rail (ground).
11	SIGIN	I/P	Signal input. The signal to this pin should be ac coupled. The dc bias of this pin is set internally.
12	V _{BIAS}	O/P	Internally generated bias voltage, held at V _{DD} /2 when the device is not in powersave mode. It should be decoupled to V _{SS} by a capacitor mounted close to the device pins. In powersave mode this pin is pulled towards V _{SS} .
13	AMPNINV	I/P	The non-inverting input to the on-chip amplifier.
14	AMPINV	I/P	The inverting input to the on-chip amplifier.
15	AMPOP	O/P	The output of the on-chip amplifier, this is internally connected to the input of the Level Detector.
16	V _{DD}	Power	The positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to V _{SS} by a capacitor.

Notes: I/P = Input
O/P = Output

1.4 External Components



C1	33pF	±20%	R1	100kΩ	±10%
C2	33pF	±20%	R2	510kΩ	±10%
C3	0.1μF	±20%	R3	20kΩ	±10%
C4	0.1μF	±20%			
C5	100pF	±20%	X1	3.579545MHz	±100ppm
C6	1.0μF	±20%			
C7	1μF	±20%			

Figure 2 Recommended External Components

1.5 General Description

1.5.1 Overall Function Description

The FX663 consists of a Call Progress Tone Detector, a 620Hz Detector and a Level Detector.

The FX663 Call Progress Tone Detector uses different tone detection methods from those commonly found with other products.

Many traditional devices use a bandpass filter followed by an energy detector. The filter is usually designed to pass input signals with a frequency between about 300Hz and 700Hz, and the amplitudes of signals in this range are then checked against a level threshold. Any signal of acceptable level in this frequency band is classed as a Call Progress tone, including signals due to speech and noise. False outputs caused by speech are a common feature with these products, and background noise may lead to a stuck "detect" output.

The FX663, by contrast, uses a stochastic signal processing technique based on analysis in both the frequency and time domain, with signal amplitude forming a small part in the decision process. This analysis includes checks on whether the signal has a "profile" which matches international standards for Call Progress tones, or a profile more likely to match that of speech, noise or other non-call-progress signals. It also adds checks on whether tones which include frequencies corresponding with the "US Busy" signals, Special Information Tones and Fax/Modem Tones have been detected.

The following glossary, sections 1.5.3 and 1.5.4, provide a simple explanation of the decoding functions and features offered by the FX663.

1.5.2 Glossary

Call Progress Tones: The single and dual frequency tones in the range 350Hz to 620Hz specified widely for call progress signalling.

Call Progress Band: The nominal range 340Hz to 700Hz within which the FX663 will detect Call Progress tones. The detection algorithm requires that the tones have the characteristics typical of Call Progress Tones.

620Hz Detection: The nominal range 590Hz to 650Hz. Single tones in this range, or dual tones having a material frequency component within this range (e.g. 480 + 620Hz) will be detected.

Non Call Progress Signal: A signal falling within the nominal range (a) 190Hz to 895Hz, but NOT within the Call Progress Band, or (b) within the nominal range 190Hz to 895Hz, but NOT meeting the DETECTION REQUIREMENTS when the signal falls in the Call Progress Band.

Subject to the duration and other characteristics of such signals, the FX663 will usually interpret these as a Non Call Progress Signal (e.g. speech or other signal activity).

Special Information Tone: The nominal frequencies 950Hz or 1400Hz or 1800Hz.

Fax/Modem Low Tone: The nominal frequency 1250Hz.

Fax/Modem High Tone: The nominal frequency 2150Hz.

Alias Response: Frequencies above 2300Hz may cause aliasing effects in the Signal Analyser. The use of a low-pass filter in the Input Amplifier, as shown in Figure 1, will help to reduce any aliasing effects.

Minimum Input Signal: The minimum signal level for the specified tone decoding performance. The lower level at which absence of an input signal will be registered is not specified. However, a separate level detector makes amplitude information available.

No Signal: A signal falling outside the nominal range 180Hz to 2280Hz or the absence of an input signal. Either will be detected as a No Signal condition.

Nominal: Subject to dynamic tolerances within the signal analysis process. Absolute values are not material or adverse to performance.

1.5.3 Block Diagram Description (Reference Figure 1)

Amplifier

The input signal is amplified by a self-biased inverting amplifier. The dc bias of this input is internally set at $\frac{1}{2}V_{DD}$. The analyser samples the call progress signal at 9.3kHz.

Call Progress Detector: Signal Analyser

The frequency range, quality and consistency of the input signal is analysed by this functional block. To be classified as a call progress signal the input signal frequencies should lie between 340Hz and 700Hz, the signal to noise ratio must be 16dB or greater and the signal must be consistent over a period of at least 145ms. These decode criteria are continuously monitored and the assessment is updated every 7ms.

620Hz Detector

The detector is designed to aid detection of "US Busy" tone. The bandwidth of the 620Hz Detector is 60Hz and the signal must be consistent over a period of at least 145ms for detection to occur. This assessment is updated every 55ms.

Control and Output Logic

This block categorises the nature of the signal into various decoded output states and controls the four outputs. See the Truth Table in section 1.5.4.

Level Detector and OPAMP

The OPAMP is configured as an amplifier with external components R1, R2, C4 and C5. The level detector operates by measuring the level of the amplified input signal and comparing it with a preset threshold which is defined inside the FX663 as shown in the detect equation.

The detector output goes to the Control and Output Logic block. The data output is gated with the level detector's output. The data output is valid only if the level detector output is true. The level detector output can be forced true by connecting AMPNINV to V_{BIAS} and connecting AMPINV to V_{SS} through a 100k Ω resistor. An interrupt is produced if the output data changes state.

The detect equation is:

$$\text{For detect level} \quad \text{Gain} \times \text{input signal level} > 250 \text{ mVp-p}$$

where gain = $-R2/R1$.

This amplifier may be used to buffer, unbalance or amplify line signals if required.

Xtal/Clock Oscillator

If the on-chip Xtal oscillator is to be used, then external components X1, R1, C1 and C2 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin and the XTALN pin should be left unconnected.

1.5.4 Decode Output Truth Table

D3	D2	D1	D0	Conditions
0	0	0	0	No Signal
0	0	0	1	Call Progress Dual Tones: Will detect 350+440, 400+450, 440+480 Hz tones
0	0	1	0	Non Call Progress Signal, e.g. Voice Activity
0	0	1	1	Call Progress Dual Tone including 620Hz Detection: Will detect 480+620 Hz tones
0	1	0	0	Special Information Tone: Will detect 950, 1400 and 1800 Hz tones
0	1	0	1	Call Progress Single Tone: Will detect 400, 425, 440 and 450 Hz tones
0	1	1	0	Will detect a single tone lying outside the Call Progress Band and within the Non Call Progress signal range
0	1	1	1	Call Progress Single Tone including 620Hz Detection: Will detect 600 and 620 Hz tones
1	0	0	0	Fax/modem High Tone: Will detect 2100 and 2200 Hz tones
1	0	0	1	Reserved for future use
1	0	1	0	Reserved for future use
1	0	1	1	Reserved for future use
1	1	0	0	Fax/modem Low Tone: Will detect 1200 and 1300 Hz tones
1	1	0	1	Reserved for future use
1	1	1	0	Reserved for future use
1	1	1	1	Reserved for future use

1.6 Application Notes

1.6.1 General

Apply a reset after power-up by taking the ENABLE pin low. This places the device in a powersave mode and resets the internal circuits. It also places the data word output (D0-D3) in a high impedance state, regardless of the level on the CSN pin.

From this mode the device can be returned to normal operation without any additional settling time, when using the component values recommended in Figure 2. The tone response times remain the same and are given in section 1.7.1.

An interrupt is produced when the decode state is changed. This interrupt is reset by CSN going to logic "0". When CSN is permanently at "0", the interrupt condition is a 5 μ s logic "0" pulse on the IRQN pin. When CSN is set to logic "1", the data word output (D0-D3) goes into a high impedance state.

1.6.2 Typical Response

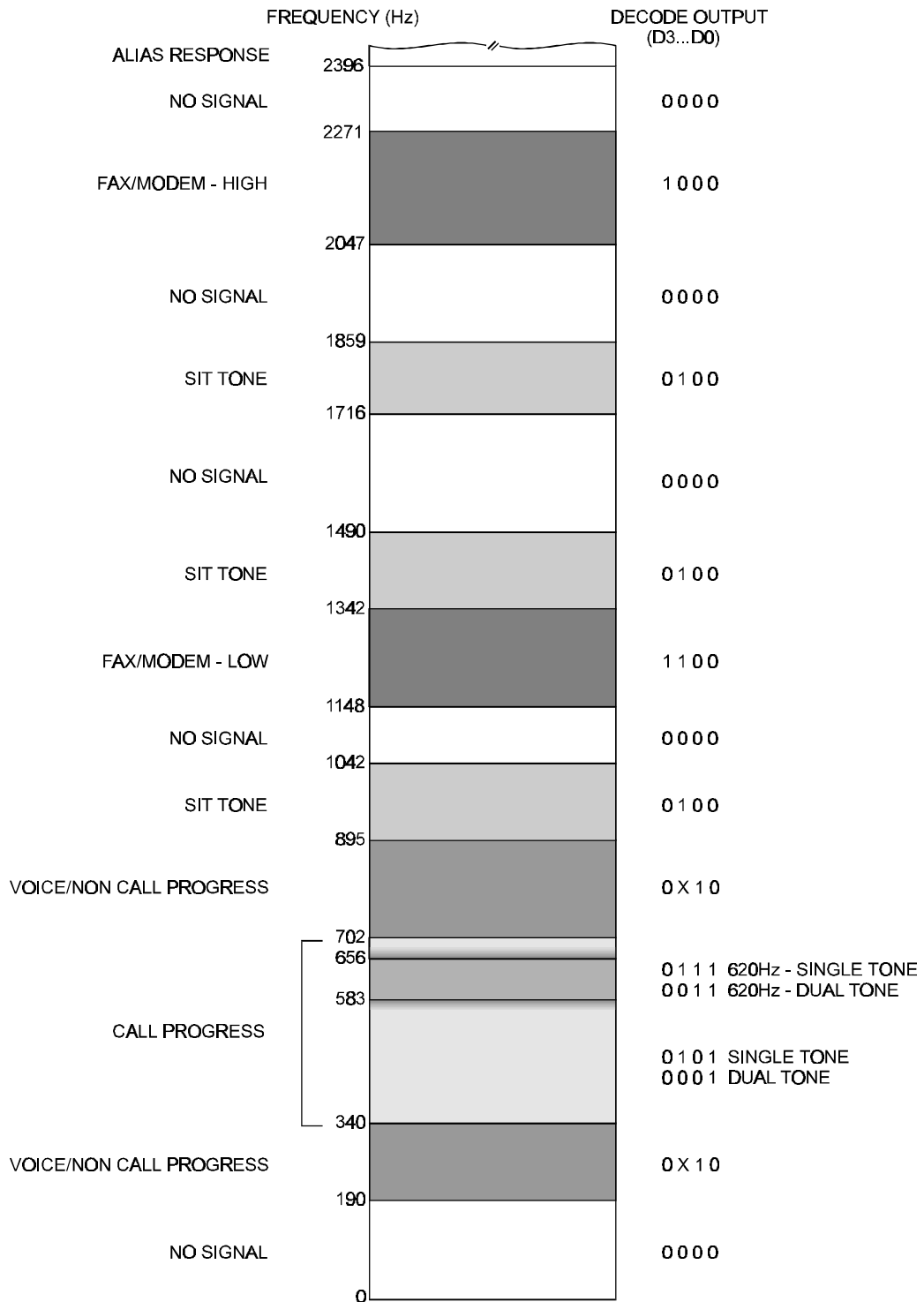


Figure 3 Typical Response Chart

1.7 Performance Specification

1.7.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply ($V_{DD} - V_{SS}$)	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	$V_{DD} + 0.3$	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

P3 and D4 Package	Min.	Max.	Units
Total Allowable Power Dissipation at $T_{amb} = 25^{\circ}\text{C}$		800	mW
... Derating		13	mW/ $^{\circ}\text{C}$
Storage Temperature	-55	+125	$^{\circ}\text{C}$
Operating Temperature	-40	+85	$^{\circ}\text{C}$

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply ($V_{DD} - V_{SS}$)		3.0	5.5	V
Operating Temperature		-40	+85	$^{\circ}\text{C}$
Xtal Frequency		3.57	3.59	MHz

Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz
 $V_{DD} = 3.3V$ to $5.0V$, $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$.
 0dB = 775 mVrms, S/N = 20dB
 Noise Bandwidth = 5kHz Band Limited Gaussian

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (all powersaved)	1, 2	-	30	-	μA
I_{DD} at $V_{DD} = 3.3V$	1	-	0.5	1	mA
I_{DD} at $V_{DD} = 5.0V$	1	-	1.0	2	mA
Logic Interface					
Input Logic '1'		70%	-	-	V_{DD}
Input Logic '0'		-	-	30%	V_{DD}
Input Leakage Current (Logic '1' or '0')		-1.0	-	1.0	μA
Input Capacitance		-	-	7.5	pF
Output Logic '1' ($I_{OH} = 120\mu A$)		90%	-	-	V_{DD}
Output Logic '0' ($I_{OL} = 360\mu A$)		-	-	10%	V_{DD}
'Off' State Leakage Current	3	-	-	10.0	μA
AC Parameters					
SIGIN Pin					
Input Impedance	4	-	0.35	-	$M\Omega$
Minimum Input Signal Level		-	-40.0	-	dB
Input Signal Dynamic Range		40.0	-	-	dB
Level Detector					
Detection Signal Level (measured at AMPOP pin)	5	-	-19.0	-	dB
OPAMP					
Input Impedance	6	10.0	-	-	$M\Omega$
Voltage gain		-	500	-	V/V
Xtal/Clock Input					
Pulse Width ('High' or 'Low')	7	40.0	-	-	ns
Input Impedance (at 100Hz)		10.0	-	-	$M\Omega$
Gain (I/P = 1mV rms at 1kHz)		20.0	-	-	dB

- Notes:**
1. Not including any current drawn from the device pins by external circuitry.
 2. Enable input at V_{SS} , CSN input at V_{DD} .
 3. IRQN pin, D0 to D3 pins.
 4. Small signal impedance over the frequency range 100Hz to 2300Hz and at 5.0V.
 5. Input signal level is multiplied by the voltage gain ($-R2/R1$). The overall signal should be larger than 250mVp-p, at $V_{DD} = 5.0V$, scale signal for different V_{DD} .
 6. Open loop, small signal low frequency measurements.
 7. Timing for an external input to the XTAL/CLOCK pin.

1.7.1 Electrical Performance (continued)

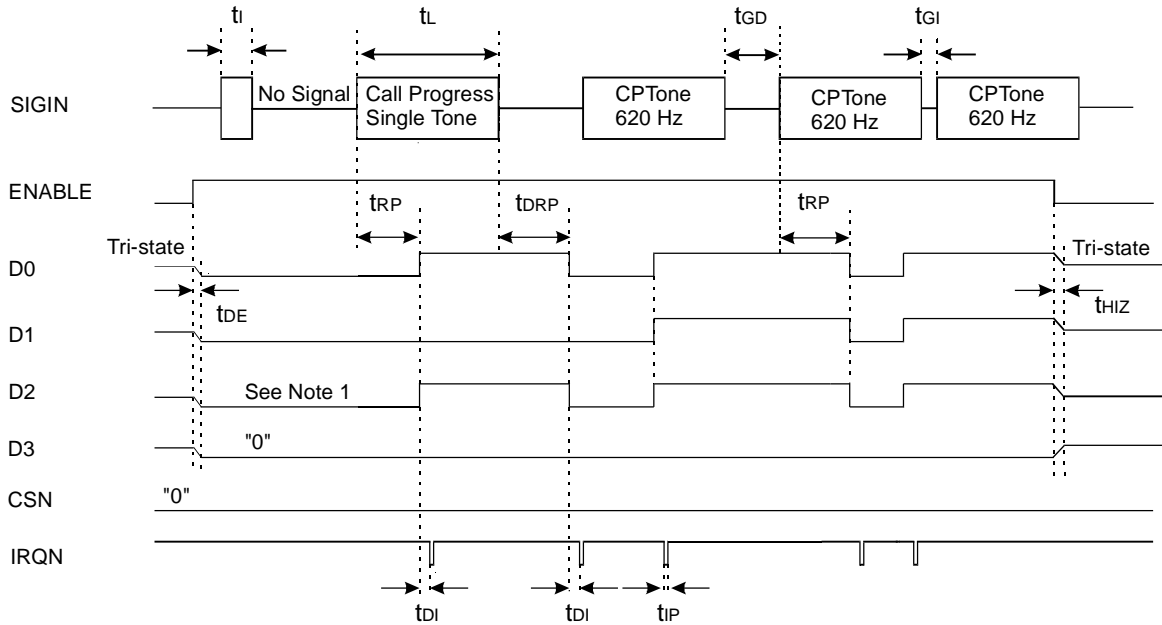


Figure 4 Timing Diagram: Call Progress Tone(s)

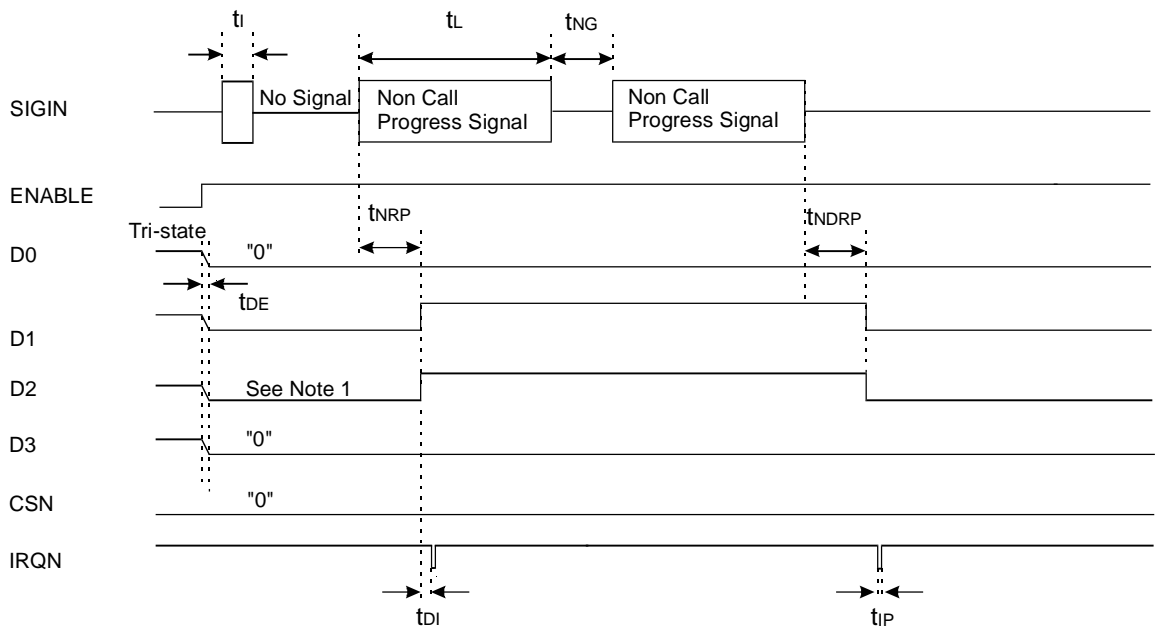


Figure 5 Timing Diagram: Non Call Progress Signal

Note 1: D2 is '1' only when the Call Progress signal, or a Non Call Progress signal, is a single frequency tone.

1.7.1 Electrical Performance (continued)

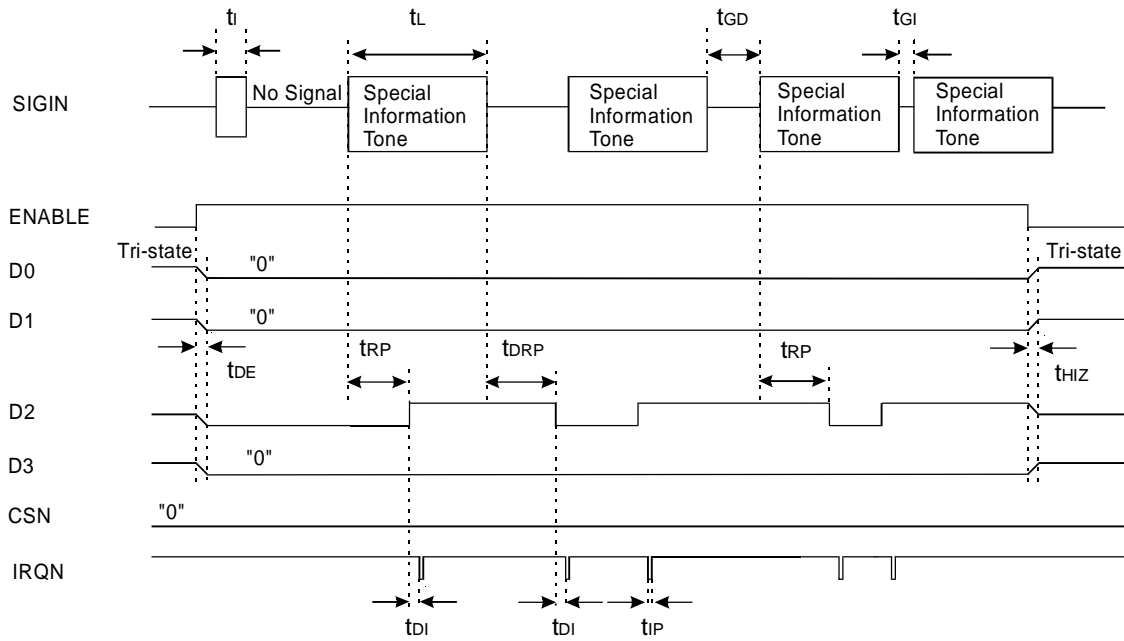


Figure 6 Timing Diagram: Special Information Tones

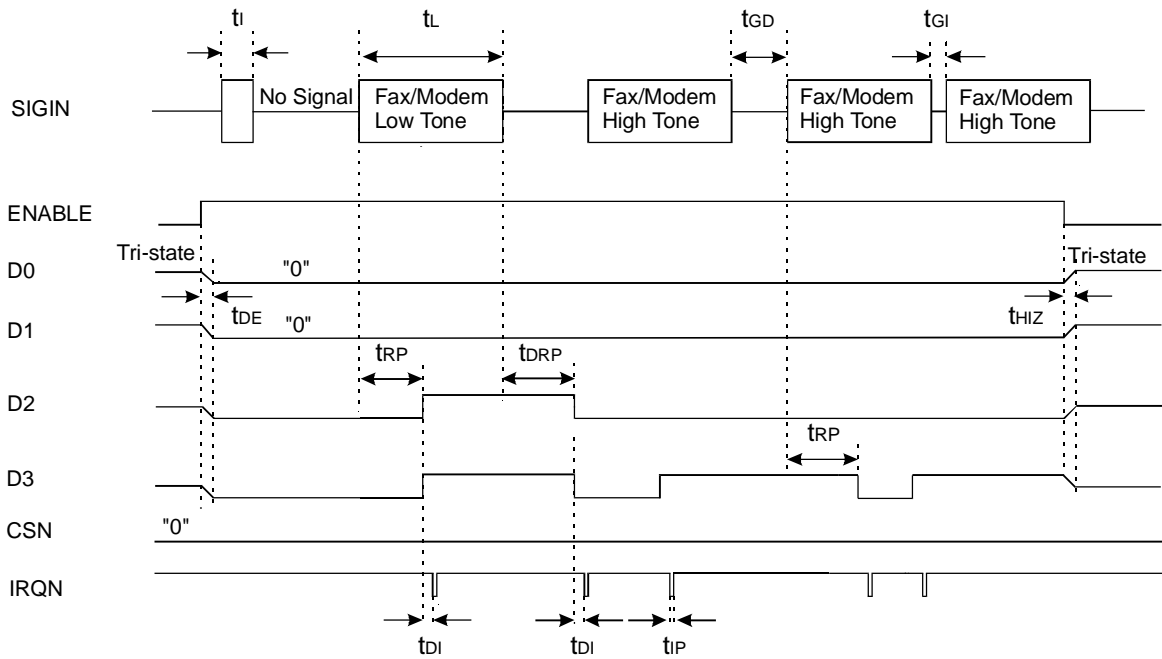


Figure 7 Timing Diagram: Fax/Modem Tones

1.7.1 Electrical Performance (continued)

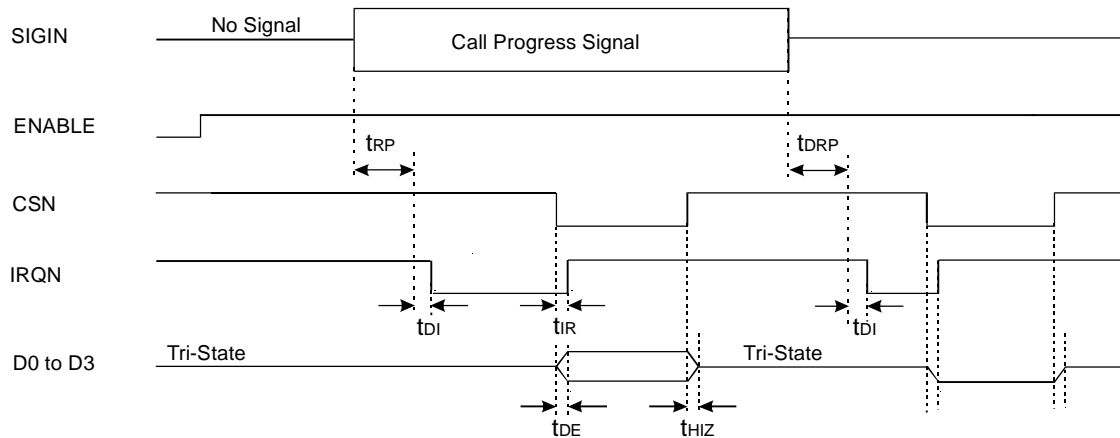


Figure 8 Bus Timing

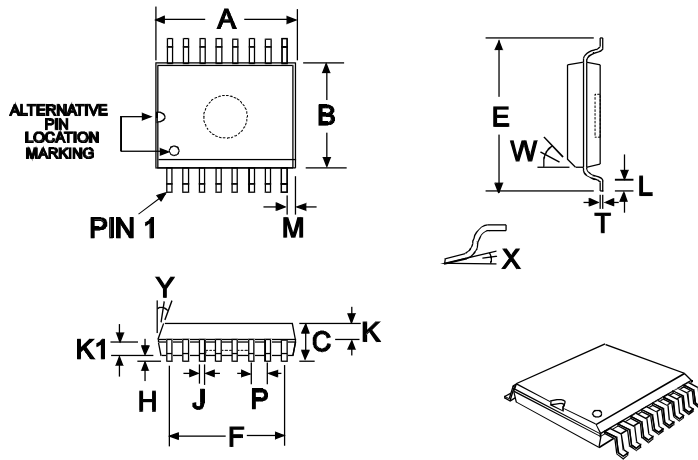
For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz, $V_{DD} = 3.3V$ to $5.0V$, $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$.

Parameter	Notes	Min.	Typ.	Max.	Units
t_{RP}	Call Progress Tone Response Time	8	-	145	ms
t_{DRP}	Call Progress Tone De-response Time	8	-	145	ms
t_{NRP}	Non Call Progress Signal Response Time	145	-	-	ms
t_{NDRP}	Non Call Progress Signal De-response Time	-	80	-	ms
t_I	Burst Length Ignored	8	-	70	ms
t_L	Burst Length Detected	8	145	-	ms
t_{GI}	Call Progress Tone Gap Length Ignored	8,9,11	-	20	ms
t_{GD}	Call Progress Tone Gap Length Detected	8,9	40	-	ms
t_{NG}	Non Call Progress Signal Gap Length Ignored	10	-	80	ms
t_{DI}	Data available to Interrupt pulse	-	-	430	μs
t_{DE}	"CSN-Low " to Data Valid	-	-	0.2	μs
t_{HIZ}	"CSN-High" to Output Tri-state	-	-	1.0	μs
t_{IR}	Interrupt Reset Time	-	-	0.2	μs
t_{IP}	Interrupt Low Pulse	4.0	5.0	6.0	μs

- Notes:**
- 8. Timing also applies to Special Information Tones and Fax/modem Tones.
 - 9. Only applies to burst of the same frequency.
 - 10. If the gap > 90ms, a NO Signal state will be detected.
 - 11. Special Information Tones and Fax/modem tones t_{GI} is 15ms maximum.

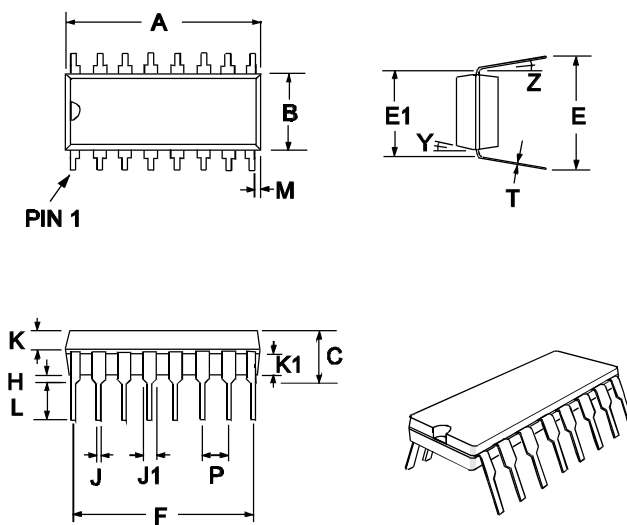
1.7.2 Packaging



DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.291 (7.39)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.394 (10.01)		0.419 (10.64)
F		0.366 (9.29)	
H	0.004 (0.10)		0.012 (0.30)
J	0.013 (0.33)		0.019 (0.48)
K		0.041 (1.04)	
K1		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
M	0.021 (0.53)		0.031 (0.79)
P		0.050 (1.27)	
T	0.009 (0.23)		0.012 (0.30)
W		45°	
X		0°	8°
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 9 D4 Mechanical Outline: Order as part no. FX663D4

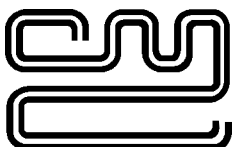


DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.260 (6.60)
C	0.135 (3.43)		0.175 (4.45)
E	0.300 (7.62)		0.390 (9.91)
E1	0.290 (7.37)		0.325 (8.26)
F		0.70 (17.78)	
H	0.015 (0.38)		0.035 (0.89)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
K1	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
M		0.028 (0.72)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 10 P3 Mechanical Outline: Order as part no. FX663P3

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.



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